IN THE CLAIMS

Please amend the claims as follows:

1. (original) A track-and-hold circuit having an input (Vin) and an output signal (Vs), a bootstrap switch (14a) having as its inputs a clock signal and an input signal (Vin), said input signal (Vin) being connected to said output signal (Vs) of said circuit via level shifting (20) and buffering means (30), characterized in that said input signal of said bootstrap switch (14a) comprises said output signal (Vs) of said circuit.

2. (original) A track-and-hold circuit according to claim 1, including two or more bootstrap switches (14a, 14b), the input signal of each of which is connected to said output signal (Vs) of said circuit via said level shifting (20) and buffering means (30).

3. (currently amended) A track-and-hold circuit according to claim 1~~ or claim 2~~, wherein said buffering means (30) comprises a MOS transistor.

4. (original) A track-and-hold circuit according to claim 3, wherein said MOS transistor (30) is a PMOS transistor.

5. (currently amended) A track-and-hold circuit according to ~~any one of claims 1 to 4~~claim 1, further comprising a capacitor (12), said input signal being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit.

6. (original) A track-and-hold circuit according to claim 5, further comprising one or more dummy switches (16) which are clocked in anti-phase to said switch (10) connecting said input signal (Vin) to said capacitor (12).

7. (original) A track-and-hold circuit according to claim 6, wherein said input signal (Vin) is connected to said dummy switches (16) via a bootstrap switch (14b), having as an additional input an anti-phase clock signal.

8. (currently amended) An analog-to-digital converter including a track-and-hold circuit according to ~~any one of claims 1 to 7~~claim 1.

9. (original) An integrated circuit including an analog-to-digital converter according to claim 8.